PCI 9030 Data Book

Version 1.0

April 2000

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PREFACE

The information contained in this document is subject to change without notice. Although an effort has been made to keep the information accurate, there may be misleading or even incorrect statements made herein.

The following is a list of additional documentation to provide the reader with more information about the PCI 9030 and related subjects:

- *PCI Local Bus Specification, Revision 2.2*, December 18, 1998
  PCI Special Interest Group (PCI SIG)
  5440 SW Westgate Drive #217, Portland, OR 97221 USA
  Tel: 800 433-5177 (domestic only) or 503 693-6232, Fax: 503 693-8344, http://www.pcisig.com
- *PCI Hot-Plug Specification, Revision 1.0*
  PCI Special Interest Group (PCI SIG)
  5440 SW Westgate Drive #217, Portland, OR 97221 USA
  Tel: 800 433-5177 (domestic only) or 503 693-6232, Fax: 503 693-8344, http://www.pcisig.com
- *PCI Bus Power Management Interface Specification, Revision 1.1*, December 18, 1998
  PCI Special Interest Group (PCI SIG)
  5440 SW Westgate Drive #217, Portland, OR 97221 USA
  Tel: 800 433-5177 (domestic only) or 503 693-6232, Fax: 503 693-8344, http://www.pcisig.com
- *PICMG 2.1, CompactPCI® Hot Swap Specification, Revision 1.0*, August 3, 1998
  PCI Industrial Computer Manufacturers Group (PICMG)
  c/o Virtual Inc., 401 Edgewater Place, Suite 500, Wakefield, MA 01880, USA
  Tel: 781 246-9318, Fax: 781 224-1239, http://www.picmg.org

Revision History

Date	Revision	Comment
3/1999	New Release	New Release PCI 9030 Preliminary Data Book, Version 0.9.
8/1999	0.90	Update.
10/1999	0.90	Initial Release Red Book.
10/1999	0.91	Update.
11/1999	0.92	Update.
12/1999	0.93	Initial Release Blue Book.
4/2000	1.0	Production Release.

PCI 9030

PCI SMARTarget™ I/O Accelerator

April 2000
Version 1.0

CompactPCI Hot Swap Ready
for Adapters and Embedded Systems

1 INTRODUCTION

1.1 FEATURES

- *PCI Local Bus Specification* v2.2-compliant 32-bit, 33 MHz Bus Target Interface Device enabling PCI Burst Transfers up to 132 MB/s
- *PCI Bus Power Management Interface Specification* v1.1 compliant
- *PCI Local Bus Specification* v2.2 Vital Product Data (VPD) configuration support
- *PICMG 2.1, CompactPCI® Hot Swap Specification,* Revision 1.0® Hot Swap *Ready* compliant
- PCI Target Programmable Burst Management
- PCI Target Read Ahead mode
- PCI Target Delayed Read mode
- PCI Target Delayed Write mode
- Programmable Interrupt Generator/Controller
- Two programmable FIFOs for zero wait state burst operation
- Flexible Local Bus runs up to 60 MHz
- 3.3/5V tolerant PCI and Local signaling supports Universal PCI Adapter designs
- Flexible Local Bus provides 32-bit Multiplexed or Non-Multiplexed Protocol for 8-, 16-, or 32-bit Peripheral and Memory devices
- Serial EEPROM interface
- Nine programmable General Purpose I/O (GPIOs)
- Five programmable Local Address spaces
- Four programmable independent chip selects
- Programmable Local Bus wait states
- Programmable Local Read prefetch mechanism
- Local Bus can run asynchronously to the PCI Bus
- Two programmable Local-to-PCI interrupts
- Endian Byte Swapping
- 3.3V Core, Low-Power CMOS in 176-pin PQFP or 180-pin µBGA
- Industrial Temp Range operation

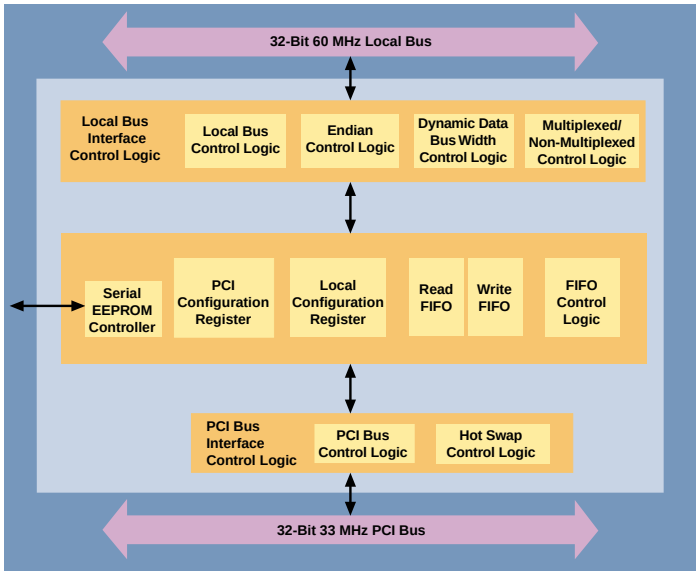

Figure 1-1. PCI 9030 Internal Block Diagram

1.2 COMPANY AND PRODUCT BACKGROUND

PLX Technology, Inc. is the world leader in PCI-to-Local Bus I/O accelerator chips, which are used in a wide variety of PCI applications. Customer applications include PCI add-in boards in PC workstations and servers, embedded PCI communication systems (such as routers and switches), and industrial PCI implementations (such as CompactPCI, PMC, and Passive Backplane PCI).

PLX Technology, Inc. is an active member of industry-standard committees, including the PCI SIG®, I_2O SIG®, and PICMG, and maintains active developer technology and cross-marketing partnerships with industry leaders, such as Intel, IBM, Hewlett-Packard, Motorola, WindRiver, and others.

Focused on providing complete solutions for PCI implementations, PLX provides design assistance to customers in the form of Reference Design and Software Development kits. Depending upon the application, these kits may include reference boards, API libraries, software debug tools, and sample device drivers, enabling customers to quickly bring new designs to production. New tools, application notes, FAQs, and information updates are frequently being added to the PLX website (http://www.plxtech.com) for customer convenience. PLX's expertise and total solutions for the PCI interface allow customers to focus on adding value in their designs without worrying about the complexities of implementing PCI and CompactPCI.

1.2.1 PCI 9030 SMARTarget I/O Accelerator

The PCI 9030, a 32-bit, 33-MHz PCI Bus Target Interface chip with SMARTarget™ Technology, is the most advanced general-purpose PCI Target device available. It offers a complete *PCI Local Bus Specification* (v2.2) implementation, enabling Burst transfers up to 132 MB/s, and is the industry's first CompactPCI Hot Swap Ready Target device. The PCI 9030 is the perfect solution for migrating legacy designs to PCI while adding new features that enhance next generation Target designs. The PCI 9030 SMARTarget I/O Accelerator brings PLX's industry-leading experience in the PCI design world to the customer in a way that is simple and convenient to use.

1.2.2 SMARTarget Technology

Many PCI chip and core designs implement only basic *PCI Local Bus Specification* v2.2 bus interface signaling, leaving the difficult performance and compatibility issues to the designer. The PCI 9030, with SMARTarget Technology, incorporates features which simplify design implementation. These features go far beyond the minimum to provide the highest possible design performance and flexibility.

SMARTarget Technology performance features:

- PCI v2.2 compliant, 32-bit, 33 MHz Target Interface, enabling PCI Burst Transfers up to 132 MB/s
- Up to 60 MHz Local Bus Operation, Enabling Burst Transfers up to 240 MB/s
- PCI Target Read Ahead mode
- PCI Target Programmable Burst
- PCI Target Delayed Write
- Posted Memory Writes

SMARTarget Technology flexibility features:

- Programmable 32-bit Local Bus operates up to 60 MHz
- Supports five PCI-to-Local Address spaces
- Nine Programmable General Purpose I/Os (GPIOs)
- Four Programmable Chip Selects
- CompactPCI Hot Swap Ready
- Big/Little Endian Byte Conversion
- Interrupt Generator/Controller
- PCI v2.2 Vital Product Data (VPD)
- *PCI Bus Power Management Interface Specification* v1.1
- 3.3/5V Tolerant PCI Signaling
- 3.3V CMOS Device in 176-PQFP or 180-pin µBGA
- Programmable Read and Write Strobe Timing on the Local Bus

1.2.3 PCI 9030 Applications

The PCI 9030 can be used in a wide variety of networking, telecom, imaging, industrial and storage applications. The PCI 9030 simplifies legacy design migration to PCI by providing a convenient off-the-shelf solution that enables prototypes to be operational in a short time period.

1.2.3.1 High-Performance PCI Target Interface

The PCI 9030's built-in SMARTarget performance features (such as 3.3/5V tolerant I/O buffers and Local Bus operation up to 60 MHz), enable designers to connect a wide variety of memory and I/O devices. With SMARTarget in action, PCI Target Adapter designs have never been simpler to implement. Figure 1-2 illustrates a typical PCI Target adapter card.

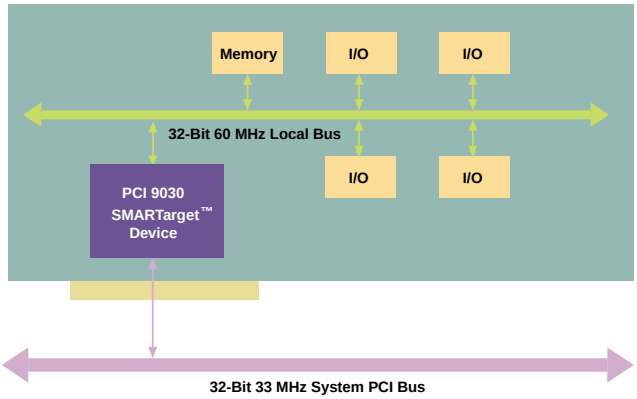

Figure 1-2. Typical PCI Target Adapter Card

1.2.3.2 High Performance CompactPCI Adapter Designs

Built upon substantial CompactPCI experience, the PLX PCI 9030 is the industry's first CompactPCI Hot Swap *Ready* Target device. This allows CompactPCI I/O board designs to be compatible with both traditional CompactPCI and new Hot Swap system designs. Figure 1-3 illustrates a typical CompactPCI adapter card.

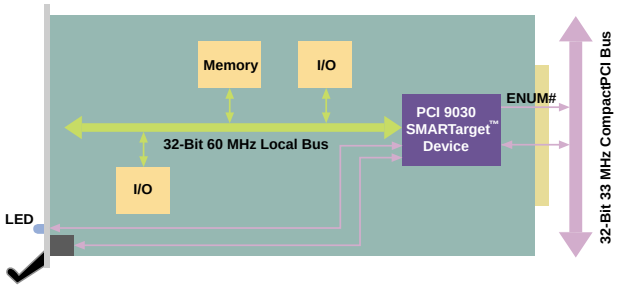

Figure 1-3. High-Performance CompactPCI Adapter Card

1.2.3.2.1 Hot Swap Ready

Hot Swap Ready performance features include:

- *PCI Local Bus Specification* v2.2
- Tolerant of Vcc from early power
- Tolerant of asynchronous reset
- Tolerant of precharge voltage
- Limited I/O pin leakage at precharge voltage
- Incorporates the Hot Swap Control/Status register (HS_CSR)
- Incorporates an Extended Capability Pointer (ECP) mechanism
- Incorporates added resources for software control of ENUM#, the ejector switch, and the status LED, which indicates insertion and removal status to the user
- Precharge 10K ohm resistor network and BIAS voltage internal to the PCI 9030
- Early power support internal to the PCI 9030

1.2.3.3 PMC Adapter Cards

In the real estate-conscious world of PMC, PC-MIP, and PCMCIA PC cards, the PCI 9030 offers an attractive packaging option with the dime-size 180-pin µBGA. SMARTarget flexibility features, such as GPIOs and Programmable Chip selects, save additional valuable board space. The PCI 9030 enables a whole new generation of mini form factor PCI cards.

Figure 1-4 illustrates a typical PMC adapter card and Figure 1-5 illustrates a typical PCMCIA PC card.

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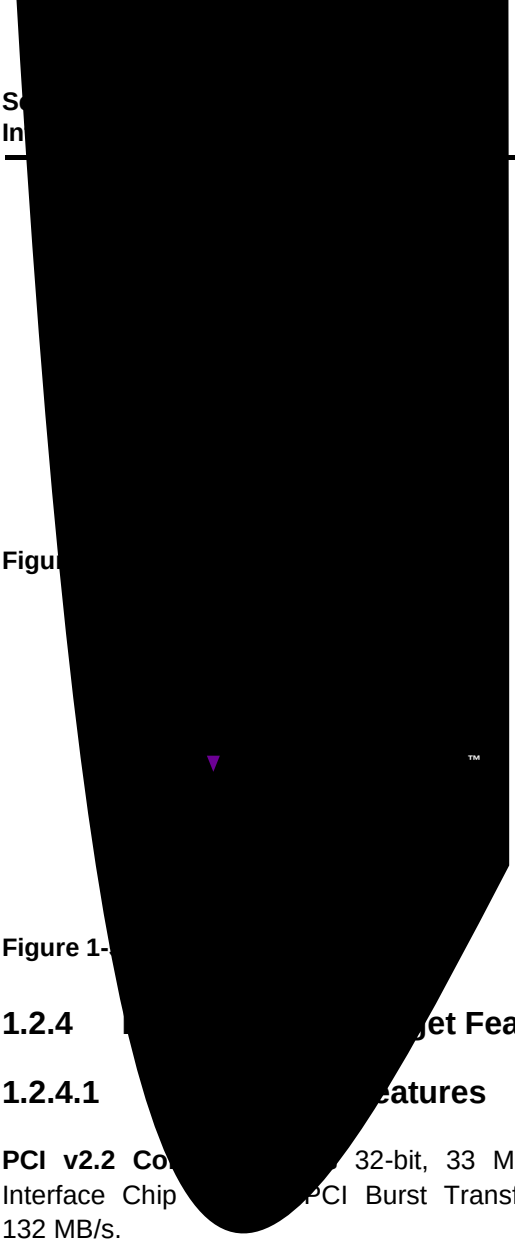

Figure 1-

1.2.4 et Features

1.2.4.1 eatures

PCI v2.2 Co 32-bit, 33 MHz Target Interface Chip PCI Burst Transfers up to 132 MB/s.

Up to 60 MHz Local Bus Operation. Enables burst transfers up to 240 MB/s.

PCI Target Read Ahead Mode. Prefetches a programmable amount of data from the Local Bus. This data can then be burst-transferred onto the PCI bus from the PCI 9030 internal PCI Target Read FIFO. The prefetch size can be programmed to match the PCI master burst length or can be used in the PCI Target Read Ahead mode data. This feature also allows for increased bandwidth and reduced read latency.

PCI Target Programmable Burst. The PCI 9030 may be programmed for several burst lengths, including unlimited burst. This allows for maximum transfer rates on both the PCI and Local Buses.

PCI Target Delayed Write Mode. The PCI Target Write data accumulates in the PCI Target Write FIFO to allow uninterrupted burst transactions on the Local Bus. This allows for a higher throughput for conditions in which the PCI Clock frequency is slower than the Local Clock frequency.

Posted Memory Writes. A PCI Memory write is posted to the PCI 9030 for later transfer to the Local

Two Programmable FIFOs for Zero Wait State Burst Operation. The following table describes the FIFO depth.

Table 1-1. FIFO Depth

FIFO	Length
PCI Target Read	16 Lwords
PCI Target Write	32 Lwords

3.3/5V Tolerant PCI Signaling. Enables Universal PCI Adapters.

3.3V CMOS Device in 176-pin PQFP or 180-pin μBGA.

1.2.4.3 Additional Features

5 Volt Tolerant Operation. The PCI 9030 requires a 3.3V supply. It provides 3.3V signaling with 5V I/O tolerance on both the PCI and Local Buses.

Serial EEPROM Interface. Contains a serial EEPROM interface that offers the option of loading configuration information from an EEPROM device.

Clocks. The Local Bus interface runs from a Local Bus clock, which runs asynchronously to the PCI clock. In addition, the PCI 9030 provides a PCI Buffered clock, which can be used as a Local Bus clock.

RST# Timing. Supports response to first configuration accesses after de-assertion of PCI RST# in less than 2^{25} clocks.

Subsystem and Subsystem Vendor IDs. Contains Subsystem ID and Subsystem Vendor ID in the PCI Configuration register space, in addition to Device and Vendor IDs. The PCI 9030 also contains a permanent Vendor ID (10B5h) and Device ID (9030h).

Silicon Revision ID. Contains the PCI 9030 Silicon Revision ID, which is programmable by way of the serial EEPROM.

1.2.5 PCI 9030 Data Assignment Convention

The following table describes the PCI 9030 data assignment convention.

Table 1-2. PCI 9030 Data Assignment Convention

Data Width	PCI 9030 Convention
1 byte (8 bits)	Byte
2 bytes (16 bits)	Word
4 bytes (32 bits)	Lword

1.2.6 PLX Chip Compatibility

1.2.6.1 Pin Compatibility

The PCI 9030 is ***not*** pin compatible with the PCI 9050, PCI 9052, PCI 9054, ***nor*** the PCI 9080.

1.2.6.2 Register Compatibility

All registers implemented in the PCI 9050 and 9052 are implemented in the PCI 9030. The PCI 9030 includes many new bit definitions and several new registers. Refer to Table 1-3 for details.

The PCI 9030 is ***not*** register-compatible with the PCI 9080 nor the PCI 9054.

1.2.7 PCI 9030, PCI 9050, and PCI 9052 Comparison

The following table compares the PCI 9030, PCI 9050, and PCI 9052.

Table 1-3. PCI 9030, PCI 9050, and PCI 9052 Comparison

Feature	PCI 9030	PCI 9050	PCI 9052
Pin Count and Type	176 PQFP/180 µBGA	160 PQFP	160 PQFP
Package Size	27 x 27 mm	31 x 31 mm	31 x 31 mm
Local Address Spaces	5	5	5
PCI Initiator Mode	No	No	No
Number of FIFOs	2	2	2
FIFO Depth—PCI Target Write	32 Lwords (128 bytes)	16 Lwords (64 bytes)	16 Lwords (64 bytes)
FIFO Depth—PCI Target Read	16 Lwords (64 bytes)	8 Lwords (32 bytes)	8 Lwords (32 bytes)
LLOCKo# Pin for Lock Cycles	Yes	Yes	Yes
WAITo# Pin for Wait State Generation	Yes	Yes	Yes
BCLKo (BCLKO) Pin; Buffered PCI Clock	Yes	Yes	Yes
ISA Bus Interface	No	No	Yes
Register Addresses	Identical to the PCI 9050 and PCI 9052, except the PCI 9030 contains additional registers related to added functionality	—	—
Big Endian ⇔ Little Endian Conversion	Yes	Yes	Yes
PCI Target Delayed Read Transactions	Yes	Yes	Yes
PCI Target Delayed Write Transactions	Yes	No	No
PCI Target Local Bus READY# Timeout	Yes	No	No
PCI Bus Power Management Interface v1.1	Yes	No	No
PCI Local Bus Specification v2.2 VPD Support	Yes	No	No
Programmable Prefetch Counter	Yes	Yes	Yes
Programmable Wait States	Yes	Yes	Yes
Programmable Ready Timeout	Yes	No	No
Programmable GPIOs	9	4	4
Additional Device and Vendor ID Registers	Yes	Yes	Yes
Core and Local Bus Vcc	3.3V	5V	5V
PCI Bus Vcc	3.3V	5V	5V
3.3V PCI Bus and Local Bus Signaling	Yes	No	No
5V Tolerant PCI Bus and Local Bus Signaling	Yes	Yes	Yes
Serial EEPROM Support	2K-, 4K-bit devices	1K-bit devices	1K-bit devices
Serial EEPROM Read Control	Reads allowed via VPD function (refer to Section 9) and CNTRL Register	Reads allowed via Serial EEPROM Control Register (CNTRL)	Reads allowed via Serial EEPROM Control Register (CNTRL)
PCI Target Read Ahead Mode	Yes	No	No
CompactPCI Hot Swap Capability	Ready	Capable	Capable